REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

Claims 1-4, 13 and 14 are allowable because none of the prior art discloses or fairly disclose a test switching circuit for a high speed data interface of an integrated circuit, or a high speed data interface within an integrated circuit, or an integrated circuit having several high speed data interfaces, comprising: a plurality of switching transistors switchable and provide a plurality of different internal test signal paths within the test switching circuit between said input pad and said output pad corresponding to a plurality of test operation modes, and in the combination as claimed.

Claim 5-12 are allowable because the prior art does not teach or fairly disclose controllable test switching circuit comprises: a first transistor connected to said termination resistor output stage of the data transmission signal path a second transistor connected between said first transistor and a reference potential node; a third transistor connected between said reference potential node and a sixth transistor; a fourth transistor connected between said first transistor and a test node; a fifth transistor connected between said test node and said sixth transistor; wherein the sixth transistor is connected to said termination resistor input stage of the data reception signal path.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ramamurthy et al. (U. S. Patent No. 5, 787, 114) discloses a loop-back test system for providing local fault detection within the integrated I/O interface device on an integrated circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AMY HE whose telephone number is (571)272-2230. The examiner can normally be reached on 9:30am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on 571-272-2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Amy He/

Primary Examiner, Art Unit 2831